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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/918,691	PRIMROSE ET AL.	
	Examiner	Art Unit	
	Clemence Han	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-41* is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☒ Claim(s) *42-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujisawa et al. (US 6,785,290).

Regarding to claim 1, Fujisawa teaches a networking apparatus comprising; a switching fabric 42 comprising a plurality of ingress/egress points capable of switching routing paths of packets received through mediums coupled to the ingress/egress points (see Figure 8D); and a first buffering structure comprising a first plurality of storage structures and a first associated packet diversion logic and a first packet insertion logic 16, said first plurality of storage structures comprising an egress diverted packet buffer 44A coupled to said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer (DQ1-DQ5 in 56) structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer 44B coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said first buffering structure coupled to a first of said ingress/egress points.

Regarding to claim 2, Fujisawa teaches said first buffering structure comprises a register interface 110, including packet unpacking logic, coupled to said egress diverted packet buffer 44A to facilitate retrieval by a processor 46 diverted ones of said egress

packets in unpacked portions (Column 1 Line 53-57), wherein the first packet diversion logic 16 is coupled to the first plurality of storage structures and further wherein the first packet diversion logic is capable of selectively routing egress packets from said first ingress/egress point to a selected one of said first plurality of storage structures (Column 11 Line 11-29).

Regarding to claim 3, Fujisawa teaches said first buffering structure comprises a register interface 110 comprising a packet packing logic capable of facilitating provision to said egress inserted packet buffer 44B by a processor 46 insertion ones of said egress packets in packed portions wherein the packet insertion logic 16 is coupled to said egress undiverted packet buffer (DQ1-DQ5 in 56) and to said egress inserted packet buffer 44B, wherein the insertion logic is capable of selectively merging undiverted ones and said insertion ones of said egress packets.

Regarding to claim 4, Fujisawa teaches a second buffering structure capable of facilitating a first plurality of ingress packets being received from a first medium into said switching fabric 42 through a second of the plurality of ingress/egress points (see Figure 8D).

Regarding to claim 5, Fujisawa teaches said second buffering structure comprises a first storage structure (DQ1-DQ5 in 66) capable of staging undiverted ones of said ingress packets; a second storage structure 44C capable of staging diverted ones of said ingress packets; a register interface 110 comprising a packet unpacking logic coupled to the second storage structure 44C, the register interface capable of facilitating retrieval by

a processor 46 said diverted ones of said ingress packets in unpacked portions (Column 1 Line 53-57) and a second packet diversion logic 64 coupled to the first medium and said first and second storage structures of the second buffering structure, wherein the second packet diversion logic is capable of selectively routing said ingress packets received from said first medium onto a selected one of said first and second storage structures of the second buffering structure.

Regarding to claim 6, Fujisawa teaches said second buffering structure comprises a first storage structure (DQ1-DQ5 in 66) coupled to said first medium capable of staging undiverted ones of said ingress packets; a second storage structure 44D capable of staging insertion ones of said ingress packets; a register interface 110 comprising a packet packing logic capable of facilitating provision to said second storage structure 44D by a processor 46 said insertion ones of said ingress packets in packed portions; and an insertion logic 64 coupled to the first and second storage structures (DQ1-DQ5 in 66, 44D) capable of selectively merging said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 7, Fujisawa teaches said second buffering structure is further capable of facilitating at least an additional undiverted one of said ingress packets being received through said second ingress/egress point, and further capable of inserting additional undiverted ones of said ingress packets into said second plurality of ingress packets (see Figure 8D).

Regarding to claim 8, Fujisawa teaches a networking apparatus comprising:

a switching fabric 42 comprising a plurality of ingress/egress points capable of switching routing paths of packets received through mediums coupled to the ingress/egress points (see Figure 8D); and a first buffering structure comprising a first plurality of storage structures and a first packet diversion logic and a first packet insertion logic 64, said first plurality of storage structures comprising an ingress diverted packet buffer 44C coupled to said first packet diversion logic and adapted to store diverted ones of ingress packets, an ingress undiverted packet buffer (DQ1-DQ5 in 66) structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of ingress packets, and an ingress inserted packet buffer 44D coupled to said first packet insertion logic and adapted to store insertion ones of ingress packets, wherein said first buffering structure coupled to a first of said ingress/egress points.

Regarding to claim 9, Fujisawa teaches said first buffering structure comprises a register interface 110 comprising a packet unpacking logic coupled to said ingress diverted packet buffer 44C, the register interface capable of facilitating retrieval by a processor 46 diverted ones of said ingress packets in unpacked portions (Column 1 Line 53-57), wherein the packet diversion logic 64 is coupled to the first medium and to the first plurality of storage structures, wherein the packet diversion logic is capable of selectively routing ingress packets received from the first medium onto a selected one of said first plurality of storage structures (DQ1-DQ5 in 66, 44C).

Regarding to claim 10, Fujisawa teaches said first buffering structure comprises a register interface 110 comprising packet packing logic capable of facilitating provision to

said ingress inserted packet buffer 44D by a processor 46 insertion ones of said ingress packets in packed portions, wherein the packet insertion logic 64 is coupled to said ingress undiverted packet buffer (DQ1-DQ5 in 66) and to said ingress inserted packet buffer 44D, wherein the packet insertion logic is capable of selectively merging undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 11, Fujisawa teaches a networking apparatus comprising: a switching fabric 42 including a plurality of ingress/egress points capable of switching packets received through mediums coupled to the ingress/egress points (see Figure 8D); and a first buffering structure comprising a first plurality of storage structures and a first packet diversion logic and a first packet insertion logic 64, said first plurality of storage structures including an ingress diverted packet buffer 66 coupled to said first packet diversion logic and adapted to store diverted ones of ingress packets, an ingress undiverted packet buffer (DQ1-DQ5 in 66) coupled between the first packet division logic and the first packet insertion logic and adapted to store undiverted ones ingress packets, and an ingress inserted packet buffer 44D coupled to said first packet insertion logic and adapted to store insertion ones of ingress packet, said first buffering structure coupled to a first of said ingress/egress points, and a second buffering structure comprising a second plurality of storage structures and a second packet diversion logic and a second packet insertion logic 16, said second plurality of storage structures including an egress diverted packet buffer 44A structurally coupled to said second packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted

packet buffer (DQ1-DQ5 in 56) coupled between the second packet diversion logic and the second packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer 44B coupled to said second packet insertion logic and adapted to store insertion ones of egress packets, said second buffering structure coupled to the first ingress/egress point.

Regarding to claim 12, Fujisawa teaches said first buffering structure comprises a divert logic 16 coupled to the first ingress/egress point and said ingress undiverted packet buffer and said ingress diverted packet buffer, the divert logic capable of selectively routing said ingress packets from said first ingress/egress point to a selected one of said ingress undiverted and diverted packet buffers (Column 11 Line 11-29); and a register interface 110 comprising a packet unpacking logic coupled to the second storage structure, the register interface capable of facilitating retrieval by a processor 46 diverted ones of said ingress packets in unpacked portions (Column 1 Line 53-57),.

Regarding to claim 13, Fujisawa teaches a register interface 110 comprising a packet packing logic capable of facilitating provision to said ingress inserted packet buffer 44B by a processor 46 insertion ones of said ingress packets in packed portions and an insertion logic 16 is coupled to said egress undiverted packet buffer (DQ1-DQ5 in 56) and to said ingress inserted packet buffer 44B, wherein the insertion logic is capable of selectively merging undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 14, Fujisawa teaches a first storage structure (DQ1-DQ5 in 66) capable of staging undiverted ones of said egress packets; a second storage structure 44C

capable of staging diverted ones of said egress packets; a divert logic 64 coupled to a first medium and said first and second storage structures of the second buffering structure, wherein the divert logic is capable of selectively routing said egress packets received from said first medium onto a selected one of said first and second storage structures of the second buffering structure; and a register interface 110 comprising a packet unpacking logic coupled to the second storage structure 44C, the register interface capable of facilitating retrieval by a processor 46 said diverted ones of said egress packets in unpacked portions (Column 1 Line 53-57).

Regarding to claim 15, Fujisawa teaches a first storage structure (DQ1-DQ5 in 66) coupled to a first medium, the first storage structure capable of staging undiverted ones of said egress packets; a second storage structure 44D capable of staging insertion ones of said egress packets; a register interface 110 comprising a packet packing logic, wherein the register interface is capable of facilitating provision to said second storage structure 44D by a processor 46 said insertion ones of said egress packets in packed portions; and an insertion logic 64 coupled to the first and second storage structures (DQ1-DQ5 in 66, 44D) capable of selectively merging said undiverted ones and said insertion ones of said egress packets.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claim 16-20, 22-27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa et al. in view of Baydar et al. (US 6,049,550).

Regarding to claim 16, Fujisawa teaches a networking module comprising; a data link/physical layer processing unit, including a buffering structure comprising a plurality of storage structures and a first packet diversion logic and a first packet insertion logic 16, said plurality of storage structures including an egress diverted packet buffer 44A coupled to said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer (DQ1-DQ5 in 56) structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer 44B coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said buffering structure coupled to a first of said ingress/egress points, the buffering structure capable of facilitating at least a selected one of data link/physical processing of ingress packets received from a medium for said packet source/sink and egress packets to be routed from said packet source/sink onto said medium, wherein each of said data link/physical processing of ingress and egress packets including at least a selected one of diversion of selected ones of a plurality of ingress/egress packets are received from/routed onto said medium, and insertion of additional ones into said plurality of ingress/egress packets being received/routed (see Figure 8D). Fujisawa, however, does not teach an optical component capable of sending and receiving optical signals encoded with data transmitted through a coupled optical medium; an optical-electrical component

coupled to the optical component capable of encoding digital data onto optical signals and capable of decoding encoded digital data on optical signals back into their digital forms; a data link/physical layer processing unit coupled to the optical-electrical component and to a packet source/sink; and a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module. Baydar teaches an optical component 265, 271 capable of sending and receiving optical signals encoded with data transmitted through a coupled optical medium; an optical-electrical component 60 coupled to the optical component capable of encoding digital data onto optical signals and capable of decoding encoded digital data on optical signals back into their digital forms; a data link/physical layer processing unit 274 coupled to the optical-electrical component 265, 271 and to a packet source/sink 267, 269; and a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module (Figure 29, Column 44). It would have been obvious to one skilled in the art to modify Fujisawa to be used in optical environment as taught by Baydar in order to be able to interface with switch systems of the future, as well as those presently in service, including analog and digital system (Column 1 Line 24-53).

Regarding to claim 17, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a divert logic 16 coupled to said packet source/sink and to said egress undiverted packet buffer (DQ1-DQ5 in 56) and to said egress diverted packet buffer 44A to selectively route said egress packets from

said packet source/sink onto a selected one of said egress undiverted packet and to egress diverted packet buffers; and a register interface 110, including packet unpacking logic, coupled to said egress diverted packet buffer 44A to facilitate retrieval by a processor 46 diverted ones of said egress packets in unpacked portions.

Regarding to claim 18, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a register interface 110, including packet packing logic, to facilitate provision to said egress inserted packet buffer 44B by a processor 46 insertion ones of said egress packets in packed portions; and an insertion logic 16 coupled to said egress undiverted packet buffer (DQ1-DQ5 in 56) and to said egress inserted packet buffer 44B to selectively merge undiverted ones and said insertion ones of said egress packets.

Regarding to claim 19, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (DQ1-DQ5 in 66) to stage undiverted ones of said ingress packets; a second storage structure 44C to stage diverted ones of said ingress packets; a divert logic 64 coupled to the medium and said first and second storage structures to selectively route said ingress packets received from said medium onto a selected one of said first and second storage structures; and a register interface 110, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor 46 said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 20, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (DQ1-DQ5 in 66) coupled to the medium to stage undiverted ones of said ingress packets; a second storage structure 44D to stage insertion ones of said ingress packets; a register interface 110, including packet packing logic, to facilitate provision to said second storage structure by a processor 46 said insertion ones of said ingress packets in packed portions; and an insertion logic 64 coupled to the first and second storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 22, Baydar teaches said data link/physical layer processing unit comprises a multi-protocol processor that is capable of supporting a plurality of datacom and telecom protocols (Column 8 Line 14-26).

Regarding to claim 23, Fujisawa teaches a processor comprising: a plurality of I/O interfaces to facilitate selective trafficking of data (Figure 8D); a plurality of data link and physical sub-layer processing units 46 selectively coupled to each other and to the I/O interfaces to be selectively employed in combination to perform selected data link and physical sub-layer processing on egress as well as ingress ones of said data, in accordance with said selected one of said plurality of protocols; and a buffering structure coupled to at least a system-side one of said I/O interfaces and a media processing one of said data link and physical sub-layer processing units, including a plurality of storage structures and a first packet diversion logic and a first packet insertion logic 16, said plurality of storage structures including an egress diverted packet buffer 44A coupled to

said first packet diversion logic and adapted to store diverted ones of egress packets, an egress undiverted packet buffer (DQ1-DQ5 in 56) structurally coupled between the first packet diversion logic and the first packet insertion logic and adapted to store undiverted ones of egress packets, and an egress inserted packet buffer 44B coupled to said first packet insertion logic and adapted to store insertion ones of egress packets, said plurality of storage structures to facilitate at least a selected one of diversion of selected ones of a plurality of egress packets, and insertion of additional ones into said plurality of egress packets, diversion of selected ones of a plurality of ingress packets, and insertion of additional ones into said plurality of ingress packets. Fujisawa, however, does not teach a multi-protocol processor comprising: a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of data transmitted in accordance with a selected one of a plurality of datacom and telecom protocols. Baydar teaches a multi-protocol processor comprising: a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of data 60 transmitted in accordance with a selected one of a plurality of datacom and telecom protocols (Column 8 Line 14-26, Figure 29, Column 44). It would have been obvious to one skilled in the art to modify Fujisawa to be used in optical environment as taught by Baydar in order to be able to interface with switch systems of the future, as well as those presently in service, including analog and digital system (Column 1 Line 24-53).

Regarding to claim 24, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a divert logic 16 coupled to said packet source/sink and said egress undiverted packet buffer (DQ1-DQ5 in 56) and to

said egress diverted packet buffer 44A to selectively route said egress packets from said packet source/sink onto a selected one of said egress undiverted packet and to egress diverted packet buffers; and a register interface 110, including packet unpacking logic, coupled to said egress diverted packet buffer 44A to facilitate retrieval by a processor 46 diverted ones of said egress packets in unpacked portions.

Regarding to claim 25, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a register interface 110, including packet packing logic, to facilitate provision to said egress inserted packet buffer 44B by a processor 46 insertion ones of said egress packets in packed portions; and an insertion logic 16 coupled to said egress undiverted packet buffer (DQ1-DQ5 in 56) and to said egress inserted packet buffer 44B to selectively merge undiverted ones and said insertion ones of said egress packets.

Regarding to claim 26, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (DQ1-DQ5 in 66) to stage undiverted ones of said ingress packets; a second storage structure 44C to stage diverted ones of said ingress packets; a divert logic 64 coupled to the medium and said first and second storage structures to selectively route said ingress packets received from said medium onto a selected one of said first and second storage structures; and a register interface 110, including packet unpacking logic, coupled to the second storage structure to facilitate retrieval by a processor 46 said diverted ones of said ingress packets in unpacked portions.

Regarding to claim 27, Fujisawa teaches said plurality of storage structures and associated packet diversion and insertion logic comprises a first storage structure (DQ1-DQ5 in 66) coupled to the medium to stage undiverted ones of said ingress packets; a second storage structure 44D to stage insertion ones of said ingress packets; a register interface 110, including packet packing logic, to facilitate provision to said second storage structure by a processor 46 said insertion ones of said ingress packets in packed portions; and an insertion logic 64 coupled to the first and second storage structures to selectively merge said undiverted ones and said insertion ones of said ingress packets.

Regarding to claim 29, Fujisawa teaches said processor is disposed on a single integrated circuit (Column 8 Line 63-64).

5. Claim 21 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa in view of Baydar et al. and further in view of Jannson et al. (US Pub. 2003/0081287).

Regarding to claim 21, Baydar teaches said optical and optical-electrical components and said data link/physical layer processing unit are capable of supporting data rates of at least 622.08 Mbps (Column 1 Line 53). Fujisawa in view of Baydar, however, does not teach said optical and optical-electrical components and said data link/physical layer processing unit are capable of supporting data rates of at least 10GB/s. Jannson teaches said optical and optical-electrical components and said data link/physical layer processing unit are capable of supporting data rates of at least 10GB/s [0026]. It would have been obvious to one skilled in the art to modify Fujisawa in view of Baydar

to support 10GB/s as taught by Jannson in order to meet the demand for high capacity communication links [0004].

Regarding to claim 28, Baydar teaches said interfaces, said plurality of data link and physical sub-layer processing unit and said buffering structure are capable of supporting data rates of at least 622.08 Mbps (Column 1 Line 53). Fujisawa in view of Baydar, however, does not teach said interfaces, said plurality of data link and physical sub-layer processing unit and said buffering structure are capable of supporting data rates of at least 10GB/s. Jannson teaches said interfaces, said plurality of data link and physical sub-layer processing unit and said buffering structure are capable of supporting data rates of at least 10GB/s [0026]. It would have been obvious to one skilled in the art to modify Fujisawa in view of Baydar to support 10GB/s as taught by Jannson in order to meet the demand for high capacity communication links [0004].

Allowable Subject Matter

6. Claim 30-41 are allowed.

7. Claim 42-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 08/24/2007 have been fully considered but they are not persuasive. In response to page 19, the applicant argues Fujisawa does not teach an egress undiverted packet buffer structurally coupled between the packet diversion logic

and the packet insertion logic. The scheduler 16 does function as the packet diversion logic (Column 7 Line 66 – Column 8 Line 1) and as the packet insertion logic (Column 8 Line 19-23) and examiner's position in the previous action was that even though the cell buffer 56 is not structurally coupled between the packet diversion logic and the packet insertion logic, it is functionally coupled between the packet diversion logic 16 and the packet insertion logic 16. However, after further consideration and discussion, examiner contends that Fujisawa's buffer 56 is structurally coupled between the diversion logic 16 and the insertion logic 16.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Friday 9 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.H.

Clemence Han
Examiner
Art Unit 2616

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